Topic No. 5

MODELING THE ENHANCEMENT OF NANOIMPRINT STAMP BENDING COMPLIANCE BY BACKSIDE GROOVES: MITIGATING THE IMPACT OF WAFER NANOTOPOGRAPHY ON RESIDUAL LAYER THICKNESS

Hayden Taylor*, Kristian Smistrup**, and Duane Boning*
* Massachusetts Institute of Technology, Cambridge, MA 02139, USA
** NIL Technology, DK-2800 Kongens Lyngby, Denmark
e-mail: hkt@mit.edu; ks@nilt.com

We describe a model for the compliance of a nanoimprint stamp with a grid of backside grooves, as proposed by Nielsen *et al.* [1]. We integrate the model with a fast simulation technique that we have previously demonstrated [2], to show how etched stamp-flexures reduce systematic, pattern-dependent residual layer thickness (RLT) variations while attenuating the contribution of random wafer nanotopography to RLT variation.

Measurements of the surface roughness of virgin silicon wafers (Fig. 1) indicate that the amplitude of nanotopography is approximately proportional to its wavelength up to scales of ≥10 mm. Nanotopography's amplitude exceeds 10% of typical target RLTs for wavelengths greater than ~1 mm, suggesting that a stamp for patterning an array of millimeter-scale chips can usefully be structured with backside grooves between the chips, allowing the stamp to conform more easily to random undulations over distances larger than a chip diameter.

Our model for the deformation of a grooved stamp incorporates local indentation, transverse shearing, and bending. We conducted a series of finite-element simulations in which we varied the flexure thickness, t_g, width, g, and initial wafer thickness, t_m. We assumed periodic boundary conditions, with uniform unit pressure applied to every ninth mesa in both directions of the stamp. A balancing uniform pressure was applied across the backside of the stamp. From these simulations we extracted the effective, 'lumped' compliance of each geometry, and fit a dimensionless model describing the considerable increase in long-range compliance enabled by backside grooves (Fig. 2). Even a gap-to-mesa-pitch ratio of 0.1 increases the compliance by ~10 times, relative to a groove-less stamp.

We have incorporated this compliance model into our nanoimprint simulation algorithm [2]. This technique describes the mechanical behavior of the resist using the response of its surface topography to a unit impulse applied at a single location. Meanwhile, deflections of the elastic stamp and substrate are described with a point-load response. The evolution of residual layer thickness is computed in a series of steps, by convolving an iteratively-found contact-pressure distribution with the scaled impulse-response of the resist. Deflections of structured stamps are described using two separate point-load response kernels: one that assumes a uniform stamp thickness of t_m and describes the relatively small deflections within the mesa, and a second kernel whose shape is piecewise-planar and captures additional relative displacements of mesas due to the presence of grooves.

Simulations using this enhanced algorithm (Fig. 3) agree closely with the experiments of Pedersen *et al.* [3]: a structured stamp with thicker material supporting the imprinted features affords far less within-chip RLT variation than a thinner stamp that can bend across the mesa. Simulations incorporating wafer nanotopographies (Fig. 4) predict that as t_g reduces, less of the nanotopography translates to mesa-to-mesa RLT variation, while systematic within-mesa RLT variation is insensitive to t_g.

This model and simulation approach could be used to optimize stamp geometries, check for interactions of differing patterns on adjacent mesas, or predict the RLT variation that will result from using a stamp or substrate with a known roughness.

Word Count: 500

References:

[1] T. Nielsen, R.H. Pedersen, O. Hansen, T. Haatainen, A. Tollki, J. Ahopelto, and A. Kristensen "Flexible Stamp for Nanoimprint Lithography," 18th IEEE Conf. MEMS 2005, pp. 508–511.

[2] H. Taylor and D. Boning, "Fast simulation of pattern dependencies in thermal nanoimprint lithography," presented at Nanoimprint and Nanoprint Technology Conf., San Jose, CA, USA: 2009.

[3] R.H. Pedersen, O. Hansen, and A. Kristensen, "A compact system for large-area thermal nanoimprint lithography using smart stamps," *J. Micromech. Microeng.*, vol. 18, 2008, p. 055018 (9pp).

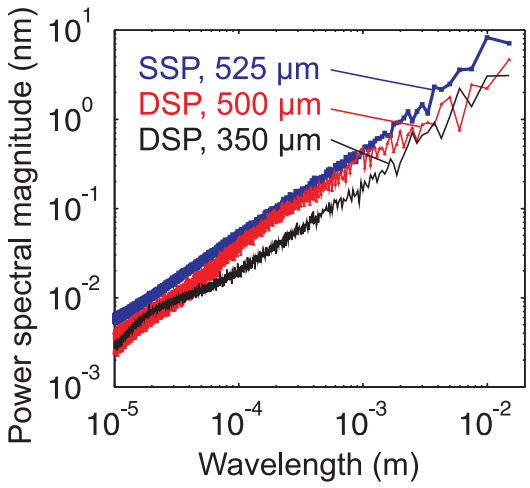

Fig. 1 Power spectra of the topographies of three different virgin silicon wafers: single-side-polished (SSP), 525 µm thick; double-side-polished (DSP) 500 µm thick; DSP 350 µm thick. Wavelengths up to approx. 13 mm are shown.

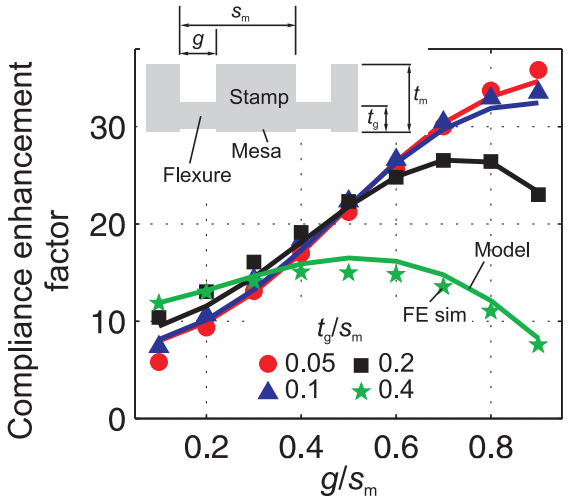

Fig. 2 Stamp compliance is considerably increased by the presence of backside grooves. 'Compliance enhancement factor' is the ratio of pk-pk deflection of the structured stamp to that of a uniformly t_m-thick stamp, under identical loadings. Symbols: finite-element simulations; lines: semi-analytical model. Inset: stamp cross-section. $t_m/t_g = 3.3$.

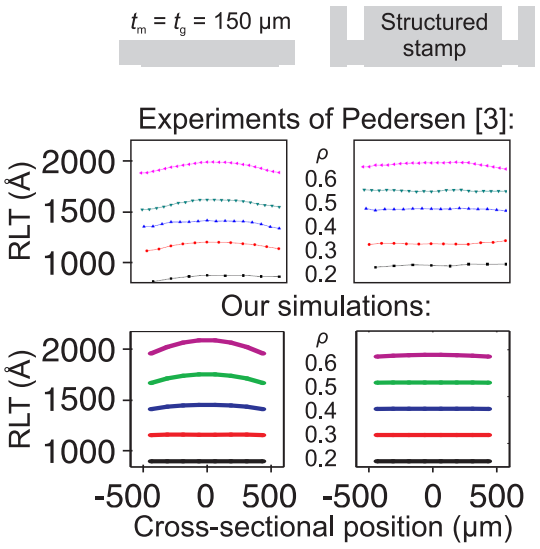

Fig. 3 A structured stamp with narrow flexures separating thicker feature-carrying mesas reduces systematic RLT variation. ρ: protrusion density. Resist viscosity fit: 2×10^5 Pa.s. $t_m = 525$ µm; $t_g = 150$ µm; $s_m = 1.5$ mm; $g = 500$ µm. Stamp-average pressure: 0.35 MPa; imprint time: 5 min.

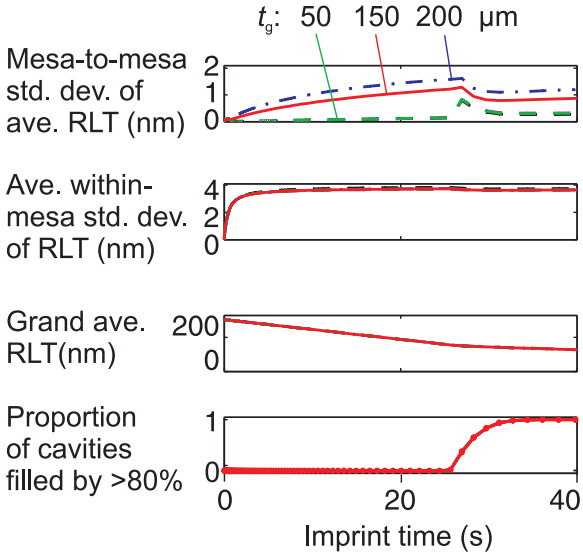

Fig. 4 Simulations of imprinting a 5×5 array of mesas into a 7.5 mm-square region. Measured wafer nanotopography (525 µm SSP wafer) was fed into simulation. Random mesa-to-mesa RLT variation reduces with smaller t_g, while systematic within-chip variation is relatively insensitive to t_g. Process as Fig. 3; $\rho = 0.3$.